On September 14, 1999, U.S. patent application serial nos. 09/396,486; 09/396,912; 09/396,203; 09/396,833; 09/396,911; 09/396,493; 09/396,487; 09/396,832; 09/396,488; 09/396,353; 09/396,834; 09/396,092; and 29/110,834 were filed. Each of these patent applications is hereby incorporated by reference herein.

~~In the claims:~~

1. (twice amended) A medical diagnostic ultrasound system subsystem having its essential data processing functionality largely residing in at least one but less than three reprogrammable logic device components.

## REMARKS

The amendments to the rewritten claim and paragraph above are shown in the attached Appendix. Underlining indicates additions, and brackets designate deletions.

In the Office Action, the Examiner rejected claims 1-77 pursuant to 35 U.S.C. §112, paragraph 1. The Examiner also rejected claims 1-77 pursuant to 35 U.S.C. §103(a) as being unpatentable over the combined teachings of Wright et al. (U.S. Patent No. 5,685,308) and Cole et al. (U.S. Patent No. 5,617,862), further in view of any of the references listed on page 4 of the Office Action. Applicants respectfully request reconsideration of the rejections.

The rejection pursuant to 35 U.S.C. §112, paragraph 1 was premised on the missing serial number information on page 66. The serial number information has been added by amendment. These serial numbers correspond to the previously listed attorney reference numbers.

A preliminary amendment was mailed on June 27, 2000. The preliminary amendment amended claims 1, 11, 31 and 34. Claims 37-45, 50, 54, 58, 62, 64, 66 and 68-77 were canceled. A copy of the amendment and the date stamped return postcard are enclosed. Please enter this amendment.

Pending claims 1-36, 46-49, 51-53, 55-57, 59-61, 63 and 67 include independent claims 1, 11, 21, 26, 31 and 34. Either the cited references are not prior art pursuant to the enclosed 37 C.F.R. §1.131 affidavit or do not disclose limitations of these claims.

Claims 1 and 11 require a subsystem essential data processing functionality largely residing in reprogrammable logic device components. As defined in the specification: "as used herein, the essential functionality comprises the function to be performed by the subsystem, such as generating a transmit waveform for a transmit beamformer subsystem or scan converting data from an acoustic grid to a display format for a scan converter. In one embodiment, the essential functionality largely (i.e. at least 40% of the processing or signal path) resides in one or more re-programmable logic devices." (page 14, lines 7-12).

Wright et al. disclose a flexible beamformer system (col. 4, lines 38-41). The beamformer is programmable, such as downloading filter coefficients and decimation factors (col. 7, lines 38-49). However, Wright et al. do not disclose reprogrammable logic device components for implementing the programmable beamformer system. As defined in the specification: "as used herein, a re-programmable logic device comprises a plurality of logic elements the gate interconnections of which can be modified by an external data set loaded under software control by a processor residing in the system. Such re-programmable logic devices include field programmable gate arrays (FPGA), flash PROM FPGA, static random access memory FPGA (SRAM FPGA) , anti-fuse programmable logic devices, complex-programmable logic devices (C-PLD), electrically erasable PLD devices and other re-programmable PLD devices." (page 13, line 27-page 14, line 2). Wright et al. do not disclose a subsystem essential data processing functionality largely residing in reprogrammable logic device components.

Cole et al. disclose using a field programmable gate array for implementing a multiplexer scheme (col. 12, lines 48-52). Various channels are switched during transmit and receive (col. 12, lines 30-48). However, the field programmable gate arrays of Cole et al. are not used for data processing, only data routing. Cole et al. do not disclose a subsystem essential data processing functionality largely residing in reprogrammable logic device components.[1]

Regarding the list of references using an FPGA, some of the references are not prior art. The inventors of the above captioned application conceived and reduced to practice the invention of claims 1 and 11 prior to the earliest claimed filing date of Inram (U.S. Patent No. 6,251,073), Smith et al. (U.S. Patent No. 6,241,675), Negrin et al. (U.S. Patent No. 6,231,510), Kemme et al. (U.S. Patent No. 6,126,608) and Gilling (U.S. Patent No. 6,126,601). These referenced did not issue more than one year before the filing date, September 14, 1999, of the above captioned application. The enclosed affidavit shows conception and reduction to practice before June 8, 1998 and thus before the filing date of these references.

The remaining references using an FPGA cited by the Examiner do not disclose a subsystem essential data processing functionality largely residing in reprogrammable logic device components required by claims 1 and 11. Doi et al. (U.S. Patent No. 5,873,824) disclose an FPGA as one possible of many components on a motherboard (col. 5, lines 40-46). The Examiner lists various devices as stated equivalents, but Doi et al. do not discuss all the listed possible devices as equivalents. Further, Doi et al. do not disclose how any FPGA is used.

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[1] See the previously submitted declarations of John Williams regarding use of FPGA's in Acuson's Sequoia ultrasound system. The Wright et al. and Cole et al. patents also disclose aspects of the Sequoia ultrasound system.

Muzilla et al. (U.S. Patent No. 5,735,797) disclose converting flow estimates to 8 bit and 4-bit outputs and applying thresholding with a output logic block (col. 6, lines 17-25). The output logic block includes a field programmable gate array which selects parameters to be displayed (col. 11, lines 13-19). The output logic block also performs median filtering of M-mode data (col. 11, lines 25-27). The output logic block is a small part of the color processing flow system (col. 4, lines 21-22; Figure 3). Muzilla et al. do not disclose using FPGA devices for the essential data processing functionality of a subsystem.

Deitrich et al. (U.S. Patent No. 5,568,813) use an FPGA for controlling interpolation by other components (col. 4, lines 56-60 and col. 5, lines 42-49). Deitrich et al. do not suggest using FPGA devices for the essential data processing functionality of a subsystem.

Likewise, Snyder (U.S. Patent No. 5,520,187) discloses using a FPGA as a logic controller (col. 5, lines 26-39). The logic controller maps the switching function of a multiplexer (col. 5, lines 50-53 and 61-65). Snyder does not disclose using FPGA devices for the essential data processing functionality of a subsystem.

Similarly, McMorrow et al. (U.S. Patent No. 5,235,985) disclose using an FPGA for multiplexing (col. 5, line 66-col. 6, line 1). McMorrow et al. do not suggest using FPGA devices for the essential data processing functionality of a subsystem.

The dependent claims 2-10, 12-20, 48-49, 51-53 and 55 depend from independent claims 1 and 11 so are allowable for the same reasons. Further distinctions over the prior art are not provided herein for brevity but will be provided if requested by the Examiner. The references using an FPGA which are not prior art to claims 1 and 11 are also not prior art for dependent claims 2-5, 8-10, 12-20, 48-49, 51-53 and 55. The inventors of the above captioned application conceived and reduced to practice the invention of claims 2-5, 8-10, 12-20, 48-49, 51-53 and 55 prior to the earliest claimed filing date of Inram, Smith et al., Negrin et al., Kemme et al. and Gilling. These references did not issue more than one year before the filing date, September 14, 1999, of the above captioned application. The enclosed affidavit shows conception and reduction to practice before June 9, 1998 and thus before the filing dates of these references.

As discussed below, none of the references cited by the Examiner disclose a reprogrammable logic device in a beamformer as claimed in claims 6 and 7.

Claims 21 and 26 require a beamformer comprising at least one re-programmable logic device. None of the cited references disclose this limitation. As discussed above, Wright et al. do not disclose reprogrammable logic device components for implementing the programmable beamformer system. Cole et al., McMorrow, and Snyder use FPGAs for multiplexing, not as a beamformer. The Examiner does not cite to a beamformer with at least one re-programmable logic device in any of the other listed references.

The dependent claims 22-25, 27-30, 56-57, 59-61 and 63 depend from independent claims 21 and 26 so are allowable for the same reasons. Further distinctions over the prior art are not provided herein for brevity but will be provided if requested by the Examiner.

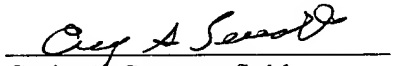
Claims 31 and 34 require a scan converter comprising at least one but less than three re-programmable logic devices. None of Wright et al., Cole et al., Doi et al., Muzilla, Deitrich et al., Snyder nor McMorrow disclose a scan converter having one to three re-programmable logic devices. Wright et al. does not disclose reprogrammable logic device components for implementing a programmable beamformer system. Cole et al., McMorrow, and Snyder use FPGAs for multiplexing, not as a scan converter. Doi et al. disclose an ultrasound system that may have an FPGA and/or other devices, not a scan converter with a re-programmable logic device. Muzilla discloses an FPGA for selecting data, but does not suggest a scan converter having a re-programmable logic device. Deitrich et al. uses an FPGA for control, not scan conversion.

The other references listed by the Examiner are not prior art to claims 31 and 34. Pursuant to the attached affidavit, the inventors of the above captioned application conceived and reduced to practice the invention of claims 31 and 34 prior to the earliest claimed filing date of Inram, Smith et al., Negrin et al., Kemme et al. and Gilling.

The dependent claims 32-33, 35-36, 65 and 67 depend from independent claims 31 and 34 so are allowable for the same reasons. Further distinctions over the prior art are not provided herein for brevity but will be provided if requested by the Examiner. The references using an FPGA which are not prior art to claims 31 and 34 are also not prior art for dependent claims 32-33, 35-36, 65 and 67. The inventors of the above captioned application conceived and reduced to practice the invention of claims 32-33, 35-36, 65 and 67 prior to the earliest claimed filing date of Inram, Smith et al., Negrin et al., Kemme et al. and Gilling. These referenced did not issue more than one year before the filing date, September 14, 1999, of the above captioned application. The enclosed affidavit shows conception and reduction to practice before June 9, 1998 and thus before the filing date of these references.

Applicants respectfully submit that all of the pending claims are in condition for allowance and seeks early allowance thereof. If for any reason, the Examiner is unable to allow the application in the next Office Action and believes that an interview would be helpful to resolve any remaining issues, he is respectfully requested to contact the undersigned attorneys at (312) 321-4200.

Respectfully submitted,



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Dated: November 28, 2001

APPENDIX

In the Specification at page 66, lines 1-10:

On September 14, 1999, U.S. patent application serial nos. 09/396,486; 09/396,912; 09/396,203; 09/396,833; 09/396,911; 09/396,493; 09/396,487; 09/396,832; 09/396,488; 09/396,353; 09/396,834; 09/396,092; and 29/110,834 [____ (attorney docket no. 9994-8US/ECTON 1), ____ (attorney docket no. 9994-9US/ECTON 2), ____ (attorney docket no. 9994-10US/ECTON 3), ____ (attorney docket no. 9994-11US/ECTON 4), ____ (attorney docket no. 9994-12US/ECTON 6), ____ (attorney docket no. 9994-13US/ECTON 7), ____ (attorney docket no. 9994-14US/ECTON 8), ____ (attorney docket no. 9994-15US/ECTON 9), ____ (attorney docket no. 9994-16US/ECTON 10), ____ (attorney docket no. 9994-7US/ECTON 11), ____ (attorney docket no. 9994-17US/ECTON 12), ____ (attorney docket no. 9994-18US/ECTON 13), and ____ (attorney docket no. 9994-19US/ECTON 14)] were filed. Each of these patent applications is hereby incorporated by reference herein.

1. (twice amended) A medical diagnostic ultrasound system subsystem having its essential data processing functionality largely residing in at least one but less than three reprogrammable logic device components.